






Method of plasma etching microminiature devices

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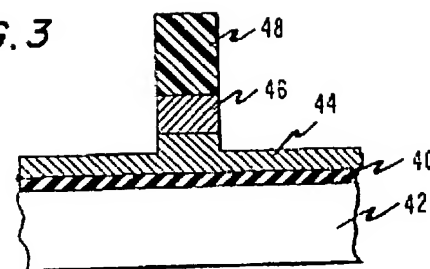
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Abstract of GB2098931

An advantageous low-resistivity gate-level metallization for VLSI MOS devices comprises TaSi₂ (46) on polysilicon (44). The two-layer composite overlies a relatively thin gate oxide film (40). In accordance with this invention, the two-layer composite is anisotropically patterned in a two-step reactive ion etching process. Patterning is carried out before the layers are sintered. In the preferred embodiment, CCl₃F is utilized to etch the TaSi₂ layer and some of the underlying polysilicon layer. Thereafter, utilizing Cl₂, the remaining polysilicon is etched in a step characterized by high selectivity with respect to the underlying gate oxide film.

FIG. 3

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